Amendments to the Specification:

Please replace paragraph [0017] with the following amended paragraph:

According to the claimed invention, a delay circuit is proposed for providing an output signal according to an input signal so that when the level of the input signal changes from a first input level to a second input level, the level of the output signal changes from a first output level to a second output level after a predetermined delay time. The delay circuit includes a voltage generator for providing a reference voltage when the input signal changes from the first input level to the second input level and a current generator for providing a charging current when the input signal changes from the first input level to the second input level. The delay circuit includes a feedback control module having a control end and two transmit ends, the control end for receiving a charging voltage ~~control signal~~, and the feedback control module able to transmit the charging current from the current generator between the two transmit ends, and the feedback control module changing the proportion between a cross voltage of the two transmit ends and the current flowing between the two transmit ends. A storage unit is electrically connected to the current generator and the control end of the feedback control module for receiving the charging current from the feedback control module and thereby generating ~~a corresponding~~ the charging voltage. ~~A feedback circuit is electrically connected between the storage unit and the control end of the feedback control module to provide the control signal according to the charging voltage.~~ The delay circuit also includes an amplifier having two input ends electrically connected to the storage unit and the ~~current~~ voltage generator in order to receive respectively the ~~reference~~ charging voltage and the ~~charging~~ reference voltage, the amplifier able to change the level of the output signal from the first output level to the second output level when the relationship between the reference voltage and the charging voltage changes.

Please replace paragraph [0034] with the following amended paragraph:

Please refer to Fig.6. Fig.6 illustrates function blocks of the delay circuit 30 in the present invention. The delay circuit 30 receives the signal Si0 as input and outputs the signal So0. It transforms the level change of the signal Si0 to the level change of the signal So0 after a delay time. The delay circuit 30 has a voltage generator 32A, a current generator 32B, a feedback control module ~~34A~~ 34, ~~a feedback circuit 34B,~~ a storage unit 36, and a differential amplifier Am.

Please replace paragraph [0035] with the following amended paragraph:

When the level of the signal Si0 changes and triggers functions of the delay circuit 30, the voltage generator 32A generates a reference voltage Vr and the current generator 32B generates a reference current Ic. Then the feedback control module 34 passes the charging current Ic to the storage unit 36 through the feedback control module ~~34A~~ 34. The storage unit 36, which can be implemented by a capacitor, provides a charging voltage Vc0 according to the charging or discharging of current Ic. The charging voltage Vc0 will be passed to ~~the feedback circuit 34B~~ a control end 37C of the feedback control module 34 and the amplifier Am. ~~The feedback circuit 34 produces a control signal Sc by the charging voltage Vc0 and this control signal Sc will feedback to a control end 37C in the control module 34A~~. The feedback control module ~~34A~~ 34 can dynamically adjust the charging current Ic passed to the storage unit 36 according to the ~~control signal Sc~~ charging voltage Vc0. At the same time, the amplifier keeps comparing the charging voltage Vc0 and the reference voltage Vr. When the comparison result between the charging voltage Vc0 and the reference voltage Vr changes during the period when the charging voltage is close to the reference voltage, the amplifier is triggered to change the level of the output signal So0 to implement the function of delay.

Please replace paragraph [0036] with the following amended paragraph:

One of the characteristics of the present invention is that the feedback control module ~~34A~~ 34 dynamically adjusts the charging current Ic passed to the storage unit 36. In practical operation, ~~when~~ the current generator 32B provides the charging current Ic and gradually changes the charging voltage Vc0 of the storage unit 36~~, the feedback circuit 34 changes the control signal Sc according to the charging voltage Vc0~~. The feedback control module ~~34A~~ 34 senses that the charging voltage Vc0 is close to the reference voltage Vr ~~by the control signal Sc~~, and it will gradually decrease the charging current Ic passed to the storage unit 36, making slower the speed in which the charging voltage approaches the reference voltage. The time when the charging voltage Vc0 reaches the reference voltage Vr is extended, and thus the delay circuit 30 implements a longer delay time. In the preferred embodiment of the present invention, the feedback control module 34 is composed of active devices (like transistors) and can reduce the large layout area of the RC circuits.

Please replace paragraph [0037] with the following amended paragraph:

Please refer to Fig.7. Fig.7 is a first embodiment of the delay circuit 40. The delay circuit 40 receives a voltage signal Vi1 as input and produces a voltage signal Vo1 as the outputs after delay. In the delay circuit 40, the resistor Ra1, Ra2 and an n-type MOSFET Qn1 form a voltage divider to implement the voltage generator 32A and produce a reference voltage Vr1 at the node Na2. Gate of the transistor Qn1 receives the trigger signal Vi1 at the node Na1. P-type MOSFET Qp2, n-type MOSFET Qn2, the inverter I1 form a current generator 42B, which generates a charging current Ic1 from the source and drain of the transistor Qp2. P-type MOSFET Qp1 is the feedback control module in the present invention. Gate is the control end, while drain and source, connected to the DC bias Vs and drain of the transistor Qp2 respectively, are ~~transition~~ transmit ends. The transistor

Qp1 controls the current Ic1 of the current generator 42B. The capacitor Ca, the storage unit of the delay circuit 40, receives the current Ic1 at the node Na3 to produce a charging voltage Vc1 at the node Na3. The connection between the node Na3 and gate of the transistor Qp1 ~~forms a feedback circuit, which~~ feeds back the voltage Vc1 to the control end of the transistor Qp1. The positive and negative inputs of the amplifier A1 (marked as "+" and "-" in Fig.7) receive the voltage Vc1 and Vr1 respectively, and generate voltage signal Vo1 as the output signal of the delay circuit 40.